[0164] Referring to FIG. **13**, a memory system **1400** may include a memory controller **1410**, and at least one memory module **1420** and **1430**, but is not limited thereto.

[0165] The memory controller **1410** may control the memory modules **1420** and **1430** so as to perform commands applied and/or transmitted from a processor, a host, etc. The memory controller **1410** may be implemented inside a processor, a host, and/or other processing device, and/or may be implemented with an application processor, a System on Chip (SoC), etc. For signal integrity, a source termination may be implemented on a bus **1440** of the memory controller **1410** through a resistor RTT. Although a VSSQ termination type of ODT is shown in the drawing, a VDD termination type of ODT control may also be performed.

[0166] In FIG. **13**, the circuit of FIG. **2** may be included in the memory controller **1410** according to at least one example embodiment.

[0167] The first memory module **1420** and the second memory nodule **1430** may be connected to the memory controller **1410** through the bus **1440**. The first memory module **1420** and the second memory module **1430** may include a plurality of semiconductor memory chips (e.g., semiconductor dies or devices) mounted onto a Printed Circuit Board (PCB), respectively, but is not limited thereto. For example, in the case of Dual In-line Memory Module (DIMM) type, the type of the memory module may be RDIMM, LRDIMM, FRDIMM, etc., but is not limited thereto. The semiconductor memory devices constituting the memory module may be divided into two or more ranks. That is, in the case of dual rank structure, a plurality of semiconductor memory devices mounted onto a board of the memory module may be classified into two ranks, and semiconductor memory devices pertaining to the same rank may be simultaneously accessed. Consequently, the rank may mean a unit by which the memory controller inputs and outputs data with respect to the semiconductor memory devices. Accordingly, when a single rank has a 64-bit data transmission width, a dual rank may have a data transmission width larger about 2 times than the single rank, and a quad rank may have a data transmission width larger four times than the single rank.

[0168] The first memory module **1420** may include at least one memory rank R**1** and R**2**, and the second memory module **1430** may include at least one memory rank R**3** and R**4**.

[0169] In at least one example embodiment of the inventive concepts, the memory ranks R**1**, R**2**, R**3** and R**4** may be connected by a multi-drop type in which data and/or address signals are transmitted and received through the same transmission line. The memory ranks R**1**, R**2**, R**3** and R**4** (i.e., the respective semiconductor memory devices included in each of the memory ranks) may be arranged in a plurality of rows, respectively and may be connected to at least one command/address register by a fly-by ring topology, a daisy chain topology, etc. Also, the memory ranks R**1**, R**2**, R**3** and R**4** may be terminated to at least one module resistor unit which provides termination resistance of Rtt/2.

[0170] In FIG. **13**, the memory system **1400** may generate a clean data strobe signal without performing a training operation, by the support of the circuit as shown in FIG. **2**. Advantageously, a delay circuit and delay control circuit which are related to delay control of the data strobe signal may not be needed. Also, since a portion of data strobe signal of the asynchronization domain can be masked without a signal training operation, the time taken (or in other words, the time required) to generate the clean data strobe signal may be shortened. Accordingly, the operation performance of the memory system **1400** may be improved.

[0171] In FIG. **13**, the semiconductor memory devices constituting the memory module have been illustrated as being implemented with volatile semiconductor memory devices (e.g., DRAM), but in other example embodiments, the volatile semiconductor memory devices may be replaced with non-volatile semiconductor memory devices (e.g., MRAM, etc.). Volatile semiconductor memory devices such as SRAM or DRAM may lose stored data when power supply is cut off. On the contrary, non-volatile semiconductor memory devices, such as Magnetic Random Access Memory (MRAM), may maintain stored data even though power supply is cut off. Accordingly, in order to prevent data being lost by power supply failure or interruption, non-volatile semiconductor memory devices may be used to store data. Additionally, when Spin Transfer Torque Magneto resistive Random Access Memory (STT-MRAM) constitutes the memory, the advantages of MRAM may be added in addition to the advantages of DRAM.

[0172] FIG. **14** is a block diagram illustrating an application example applied to a computing system according to at least one example embodiment.

[0173] Referring to FIG. **14**, a computing system **1500** may include a processor **1510**, a system controller **1520**, and a memory system **1400**.

[0174] The computing system **1500** may further include a processor bus **1530**, an expansion bus **1540**, an input device **1550**, an output device **1560**, and a storage device **1570**. The memory system **1400** may include at least one memory module **1420** and a memory controller for controlling the memory module **1420**. The memory controller **1410** may be included in the system controller **1520**.

[0175] The processor **1510** may execute various computing functions like execution of specific software which executes specific calculations or tasks. For example, the processor **1510** may be a microprocessor, a Central Processing Unit (CPU), etc. The processor **1510** may be connected to the system controller **1520** through the processor bus **1530** including an address bus, a control bus, and/or a data bus.

[0176] The host interface between the processor **1510** and the system controller **1520** may include various protocols for performing data exchange. For example, the system controller **1520** may be configured to communicate with a host or an external device through at least one of various protocols such as Universal Serial Bus (USB) protocol, MMC (multimedia card) protocol, peripheral component interconnection (PCI) protocol, PCI-Express (PCI-E) protocol, Advanced Technology Attachment (ATA) protocol, Serial-ATA protocol, Parallel-ATA protocol, Small Computer Small Interface (SCSI) protocol, Enhanced Small Disk Interface (ESDI) protocol, Integrated Drive Electronics (IDE) protocol, etc.

[0177] The system controller **1520** may be connected to the expansion bus **1540** such as a Peripheral Component Interconnect (PCI) bus. Thus, the processor **1510** may control at least one input device **1550** such as a keyboard or a mouse, at least one output device **1560** such as a printer or